ECE 745 : ASIC Verification  
Fall 2007  
Course Overview & Policies

Class Schedule: Tues, Thurs, 11.05 am to 12.20 pm, EB2-1231

Instructor: Dr. Meeta Yadav (prime instructor), Prof. Paul D. Franzon, Dr. Yadav Office Hours: Tues, Thurs, 12.30 to 1.30, EB2-2116 E-mails: {myadav, paulf}@ncsu.edu Home pages : www.courses.ncsu.edu/ece745/ www.ece.ncsu.edu/erl/faculty/paulf.html

TAs:


Prerequisite: ECE 520 ASIC Design or equivalent.

Course Objectives
1. To prepare the student to be an entry-level industrial standard cell ASIC verification engineer.
2. To give the student an understanding of issues and tools related to ASIC verification, with a focus on the methodologies supported by the SystemVerilog language.

Course Outcomes
1. Students will be able to verify a complex digital functional block, finding most of the contained bugs, using SystemVerilog.
2. Students will demonstrate an understanding of the basic methodologies used in ASIC Verification and their implementation using SystemVerilog.

Course Approach:
The course approach will be more along the lines of how a professional will learn a new skill, rather than how a student normally learns a course. The “lectures” will be used to integrate lab and book material. You will be expected to study the textbook yourself. There will be two projects. One small one to establish your skill set, another, larger one, to evaluate your capability. There will be scheduled office hours in an EOS lab for you to get help. This will be a much less structured experience than ECE 520. You WILL be expected to cope with some ambiguity, to teach yourself from available materials, and be able to work things out for yourself. There will be tests on the book chapters and one formal examination. Please note that verification, SystemVerilog and the associated tools are VERY new. There will be problems, etc. that will have to be overcome as they occur.

Student Evaluation

<table>
<thead>
<tr>
<th>Item</th>
<th>Contribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chapter Tests + Midterm</td>
<td>15%</td>
</tr>
<tr>
<td>Labs</td>
<td>20%</td>
</tr>
<tr>
<td>Project 1</td>
<td>20%</td>
</tr>
<tr>
<td>Project 2</td>
<td>30%</td>
</tr>
<tr>
<td>Final</td>
<td>15%</td>
</tr>
</tbody>
</table>

The first chapter test will be held in week 4 or soon thereafter. The tutorials and project 1 will be learning exercises. Project 2 and the midterm will be the major evaluation exercise of the class. There you will be measured against objective standards. All exercises and projects will be done individually. All tests are open book/open-notes. The audit requirement is to complete the first project to a B standard or better. Please note that it is easy to detect cheating in a project like this. Though collaboration (sharing ideas and concepts) is encouraged, sharing of code is strictly forbidden.


**Topic Covered**

1. System Verilog Verification Guidelines
2. System Verilog Data Types
3. Procedural Statements and Routines
4. Interfaces and Clocking blocks
5. Object Oriented Programming
6. Randomization
7. Threads and Interprocess Communication
8. Coverage
9. Assertions

**Students with disabilities**
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. [http://www.ncsu.edu/provost/offices/affirm_action/dss/](http://www.ncsu.edu/provost/offices/affirm_action/dss/) For more information on NC State's policy on working with students with disabilities, please see [http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html)

**Academic integrity**
All the provisions of the [code of academic integrity](http://www.ncsu.edu/provost/academic_policies/integrit/reg.htm) apply to this course. In addition, it is my understanding and expectation that your signature on any test or assignment means that you neither gave nor received unauthorized aid.

In addition, please feel free to provide anonymous feedback during semester using wolfware.