NC STATE UNIVERSITY

ECE 464/564: Digital ASIC and FPGA Design with Verilog
Course Overview & Policies
Fall 2024

Instructor: Professor Paul D. Franzon, Ph.D.
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Class Web Site: Moodle site. https://moodle-courses2425.wolfware.ncsu.edu/course/view.php?id=2187

Class Schedule:

- **Class:** 6 – 7.15 pm Monday and Wednesday in Hunt Auditorium. The class will be broadcast to the overflow room.
- **You have something due almost every Wednesday at 11:55 pm ET. (Except for the first day of class.)** Please check the class schedule near the top of the Moodle page.
- **Office Hours:** 4-5 pm Mondays and Wednesdays in EB2 3014B, and via zoom. Students in the room will generally have priority over zoom attendees. https://ncsu.zoom.us/j/93691261928?pwd=RG9zdW9pdEN6SWJCZFNTUU1HdVJuQT09 . Not every session will be held. The class calendar will specify when.

Class Format: This is a "flipped" synchronous/asynchronous class. Content is recorded on YouTube. Low stakes quizzing is used to reinforce knowledge. Classes are used to focus on how to design. Classes are recorded and broadcast using Panopto.

Communications: Students are strongly encouraged to use the Forums for questions that are not considered "private". If the question is a good discussion topic, or one that a peer can answer, myself and the TAs might not specifically respond unless it is clear the discussion is not solving it. However, if it is clear that the questions can only be answered by one of us, we will do so as soon as practical. TA Labs should be used for problems related to CAD tool and code debug issues. *I recommend you set up Moodle so that you are automatically subscribed to all forum posts. You do this in "forums" in the top right of the moodle page click on that and then click on "subscribe tto all"*

Labs. The TAs can be consulted during scheduled lab sessions and online, e.g. via Zoom. You will find these consultations very useful for resolving design and tool questions and should be your primary method to do so.

Textbooks & Notes:

Purchase is Optional. Dally and Harting is my favorite. Harris and Harris is good for fundamentals.

- M.D. Ciletti, "Advanced Digital Design with the Verilog HDL," 2nd edition, (Prentice Hall), 2010. ISBN 978-0136019282. This text is a good language guide with numerous examples.
- W. Dally and R.C. Harting: "Digital Design: A Systems Approach", (Cambridge), 2012, ISBN 0521199506
- Course notes, etc. on class web page.
- References:
  - David Money Harris and Sara L. Harris, "Digital Design and Computer Architecture". The 2007 edition is available for download for free from NC State Library.
  - Peter Wilson, "Design Recipes for FPGAs", is also available for free download from the library.
  - Thomas and Moorby, ``The Verilog Hardware Description Language", 3rd edition, Kluwer Academic. ISBN 0-7923-9723-1.
  - S. Sutherland, S. Davidman, P. Flake, "System Verilog for Design" (Kluwer), 2004, ISBN 1-4020-7350-8.
  - S. Kilts, "Advanced FPGA Design", (Wiley), ISBN 978-0-05437-6
  - H. Bhatnagar, "Advanced ASIC Chip Synthesis Using Synopsys Design Compiler, Physical Compiler, and PrimeTime", ISBN 0-7923-7644-7.

I posted an announcement on the announcement forum earlier this week. That should have resulted in an email to you. If you did NOT receive this email, check your "official" email address at www.ncsu.edu under "directories" in the top right corner, and update it if need be.

Prerequisite: Grade of C or better in ECE 212 or equivalent. ECE 310 is useful but not assumed. Functionally, I assume that students are familiar with logic design, including combinational logic gates, sequential logic gates, timing design, Finite State Machines, etc. If you have never designed and verified even a small digital circuit, and remember the principles by which they work, you will be seriously disadvantaged in this class. I do not assume knowledge of Verilog.

Course Objectives

1. To prepare the student to be an entry-level industrial standard cell ASIC or FPGA designer.
2. To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation, including timing, performance and power optimization, verification and manufacturing test.

Course Outcomes

1. Students will be able to demonstrate the design and synthesis of a complex digital functional block, containing over 1,000 gates, using Verilog HDL and Synopsys Design Compiler and an FPGA synthesis tool.
2. Students will demonstrate the formulation of a plan of how to optimize the performance, area, and power of a complex digital functional block, and the tradeoffs between these.
3. Students will be able to describe issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, impact of memories, as well as the impact of technology scaling on ASIC design.

Course Approach:

Recorded Lecture Materials: Designed to prepare you for the project and cover issues important to ASIC designers.
Classes: Classes include design and exercise activities designed to help you achieve the application level of learning. These are found at the top of the moodle page.
Laboratories: Consultation can be set up via email.
Quizzes: There are two levels of quizzes built into the pre-recorded material. Each module is broken into small segments with a quiz at the end of each segment. This quiz is simply to provide you with feedback on the knowledge and understanding you gained in that segment. Though your scores are recorded for grade, they are not a major part of your grade. There is an additional quiz at the end of each module. This score is also recorded and DOES become a significant part of your grade.
Homeworks: The homeworks are designed to either help you gain the skills required for the project or to help prepare you for the exams. Collaboration is encouraged though each student is expected to turn in individual solutions.
Project: A fixed project will be published for the class. The project will be executed individually.
Written Exams : There will be two written exams, a 75 minute midterm and a three hour final. Both are comprehensive, open-book, open-notes exams. They will be un-proctored Moodle administered exams.

Course Syllabus

0. Revision of Digital Design
1. Introduction to ASIC design
2. Timing design
3. Design of digital hardware using Verilog HDL I
4. Design of digital hardware using Verilog HDL II
5. Design of Finite State Machines
6. Design of complex systems. Reset strategies. System Verilog
7. Managing hierarchy.
8. Verification.
9. Examples, tips and techniques.
10. Design for Test.
11. Low Power Design.
12. Introduction to FPGAs
13. Memories

Homework TurnIn

- Upload to Moodle

Midterm and Final

- An unproctored timed exam will be arranged (75 min for midterm, 150 min for final. But you are still expected to do the exam on your own unassisted. The exams will be Moodle administered with highly randomized

Server Access

- You will need remote access to our Linux compute servers (and know how to work in Lunux). See "remote computing access" in the Resources module. I suggest getting remote access (via Mobaxterm or fastx) set up early. Remote access is also covered in Tutorial 1.

Student Evaluation

Item	**Date**	
Homeworks & End of module quizzes	Every Wednesday at 11.55 pm	25%
Intra module quizzes	Every Wednesday at 11.55 pm	5%
Midterm Exam	Monday, October 21, 6 – 7.15 pm	12%
Project Plan – Prelim Report	Wednesday, October 30	3%
Project – Final Report	Monday, November 11	30%
Final Exam	Monday, Dec. 6. 7.00 – 9.30 pm	25%

For EOL students, the exam window will be the day after the on campus exam.

Due to a shortage of TAs, homeworks will only be graded for submission. They wont be fully graded.

On campus students are required to come to exams. They will be held in the Hunt Auditorium.

The project item can be submitted up to one week late with a **5% penalty**. It can be submitted two weeks late with a **10% penalty**. After that it won't be accepted. Though you can collaborate during homeworks and project, **direct copying of solutions, in part or in whole, is not permitted. All code required for the homeworks and projects should be individually designed and developed**. We will be running code comparison tools on homework solutions, and projects. **Electronic sharing of code is expressly forbidden.**

Use of **AI code generation tools is permitted.** However, further sharing of such code is not. Any code authored or coauthored by AI tools should be clearly labelled by comments. Your report need to include the question chains and an explanation of how AI was used.

An Audit requires completing all the end of module quizzes and homeworks with a grade of at least 80%.

Letter grades will be determined based on demonstrated class performance against the standard of being ready to design and understand key issues upon completing the course. However, the breakpoints between letter grades will not be higher than the University defaults (e.g. 93% for an A) and will probably be lower.

EOL Students

EOL students enrolled in a 601 section will be expected to watch the Youtube and Panopto videos and to meet the same due dates as on campus students. The exception are exams. You can choose to take the exam the next day after the scheduled time. The exam will be open for 24 hours for that day.

Important Dates

See Class Schedule

Instructor Research Interests

- Application specific processors and sensor systems. Current projects are in applications of 3DICs, cortical and machine learning applications, sensor system design, and secure IP design.
- Electronic Design Automation using Machine Learning.
- Quantum Computing applications

- Interconnect, including transceivers, electronic packaging, on-chip interconnect, and between-chip interconnect.
- RFID applications and circuits.
- Advanced packaging – its design and design enablement.

Students with disabilities
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. http://www.ncsu.edu/provost/offices/affirm_action/dss/ For more information on NC State's policy on working with students with disabilities, please see http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html

Academic integrity
All the provisions of the code of academic integrity apply to this course. In addition, it is my understanding and expectation that your submission of any test or assignment means that you neither gave nor received unauthorized aid. **My policy for homeworks and projects is that while you are free to collaborate, sharing of design data, specifically Verilog code, is expressly forbidden. If you collaborate on a design problem, I still expect you to turn in individually developed code. We will run code comparison tools on the projects and some homeworks.**

In addition, do not download and reuse publicly available codes in the project, e.g. codes on githubs.
I am aware that solutions to most of the quizzes and homeworks are publicly available. If you over rely on these you will be under prepared for the project and exams which are new each year. If you turn in homework solutions for code problems that are largely identical to my solutions or that of others you will be penalized.

Discussion Forum Policy
The forums provided for this class are for technical discussion **only** about class content, including clarification of quiz questions and answers. Any other discussion is expressly forbidden. This includes discussion on class policies and extended debates about question partial/no credit once the issue is decided by the instructor. Any class policy concerns should be directly communicated with the instructor and not on a forum. Any violations will lead to removal of forum privileges. Repeat violations will result in disciplinary action being taken.

Courtesy Policy
All interactions between students and between students and instructional staff are to be courteous, and stick to the facts of the issue being discussed, even if you simply agree to disagree. Any form of character attack, and other examples of discourteous behavior will not be tolerated. Cyberbullying will not be tolerated. Disruptive behavior in class will result in removal from class. Discourteous behavior on the forum will result in removal of forum privileges. Mass or group emails will not be used by students in the context of this class. Repeat violations will result in disciplinary action being taken.

Academic Grievance Policy in COE
http://www.engr.ncsu.edu/academics/grad/policies

Student Ombudsman
http://ombuds.dasa.ncsu.edu/