

CSC/ECE 506: Architecture of Parallel Computers

Summer 2026

CSC/ECE 506

ANNOUNCEMENTS

SYLLABUS

COURSE SCHEDULE

MOODLE

EXPERTIZA

COURSE OVERVIEW

The need for parallel and massively parallel computers. Taxonomy of parallel computer architecture, and programming models for parallel architect...[More](#)

INSTRUCTOR

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TEACHING ASSISTANT

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SYLLABUS: OVERVIEW

OVERVIEW

HOMEWORK & TESTS

ACADEMIC INTEGRITY

Catalog Description

The need for parallel and massively parallel computers. Taxonomy of parallel computer architecture, and programming models for parallel architectures. Example parallel algorithms. Shared-memory vs. distributed-memory architectures. Correctness and performance issues. Cache coherence and memory consistency. Bus-based and scalable directory-based multiprocessors. Interconnection-network topologies and switch design. Brief overview of advanced topics such as multiprocessor prefetching and speculative parallel execution.

Learning Objectives

The goals for this course are to ...

- understand the problem of race conditions in concurrent systems,
- learn how to decompose a program for parallel execution,
- be able to write simple parallel programs in the important programming models,
- understand the operation of common cache-coherence algorithms, both bus-based and network-based, and
- learn about common memory-consistency models, and appreciate the advantages and disadvantages of each.

The Staff

Instructor

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Teaching Assistant

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Important dates

- First Class: Wednesday, May 15
- Last Class: Friday, July 26
- No class: Monday, May 27 (Memorial Day)
Monday, June 19 (Juneteenth)
Friday, July 5 (Independence Day, observed)
- Last day to drop or change to audit: Tuesday, June 25
- For more details, see the [academic calendar](#).

Catalog entry

- [CSC/ECE 506](#) :Architecture of Parallel Computers

Text

REQUIRED

Fundamentals of Parallel Multicore Architecture: Multichip and Multicore Systems

by Yan Solihin

Publisher: CRC Press

Pub. Date: August 2016

Prerequisites

- **CSC 312** :Computer Organization and Logic **or**
- **CSC 456** :Computer Architecture and Multiprocessors **or**
- **ECE 310** :Design of Complex Digital Systems

Online format

This course will be offered in an asynchronous online format. Before each class, students are required to read a section from the textbook and pass a short quiz on it. Classes themselves consist of several short (approximately 5- to 10-minute) videos with embedded quizzes.

Attendance requirement

Educational research shows that students learn best incrementally, rather than by studying large amounts of material right before exams. Incremental learning can only take place when students concentrate on each lesson when it is presented.

Accordingly, all students in CSC/ECE 506 are required to "attend" at least 25 out of the 26 (non-review) class sessions. Attendance credit is earned by completing the embedded quizzes in the lecture videos. Answers will not be checked; credit is obtained simply for submitting answers.

Please note that these quizzes are separate from the "pre-quizzes," described on the next page, which should be attempted after doing the reading for the class.

A student who fails to earn attendance credit for 25 class sessions will be penalized 0.5 percent on his/her final average for each class short of 25 in which (s)he earned credit.

Audit requirement

"Attend" at least half of the classes. Also, do one homework, or take one test (not pre-quiz), before fall break and score at least 50%; then do one homework, or take one test (not pre-quiz), after fall break and score at least 50%. You can choose which homework or test to take, and if you take one and fail to score 50%, you can try another. If you complete this requirement, you will receive a grade of AU. If you do not fulfill this requirement, your grade will be NR (no recognition).